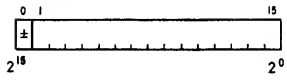
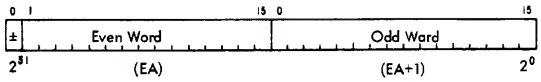
IBM 1800 Reference Card

File No. 1800-85
Form X26-5624-1
Printed in U.S.A.

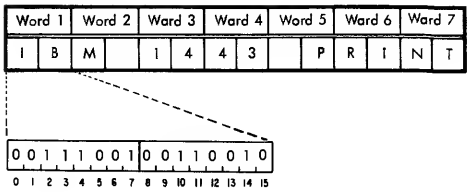
Single Precision Data Word Format



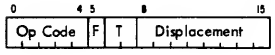
Double Precision Data Word Format



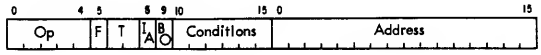
1443 Printer Core Storage Word Format



One-Word Instruction Format



Two-Word Instruction Format



1816 Keyboard and 1442 Card Image Character Coding

Key	Hex	Keyboard Entry or Card Image Bits 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	IBM Card Code
*	4220	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	11,8,4
/	3000	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0,1
0	2000	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1000	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
2	0800	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	2
3	0400	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	3
4	0200	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	4
5	0100	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	5
6	0080	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	6
7	0040	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	7
8	0020	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	8
9	0010	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	9
$	4420	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	11,8,3
	8420	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	12,8,3
,	2420	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0,8,3
EOF	0008	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	None
ER CHR	0004	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	None
ER FLD	0002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	None
=	00A0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	6,8
'	0120	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	5,8
(	8120	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	12,5,8
)	4120	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	11,5,8
+	80A0	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	12,8,6
-	4000	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	11
A	9000	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12,1
B	8800	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	12,2
C	8400	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	12,3
D	8200	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	12,4
E	8100	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	12,5
F	8080	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	12,6
G	8040	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	12,7
H	8020	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	12,8
I	8010	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	12,9
J	5000	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	11,1
K	4800	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	11,2
L	4400	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	11,3
M	4200	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	11,4
N	4100	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	11,5
O	4080	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	11,6
P	4040	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	11,7
Q	4020	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	11,8
R	4010	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	11,9
S	2800	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0,2
T	2400	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0,3
U	2200	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0,4
V	2100	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0,5
W	2080	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0,6
X	2040	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0,7
Y	2020	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0,8
Z	2010	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0,9
Space	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Blank
¢	8820	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	12,8,2
<	8220	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	12,8,4
!	8060	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	12,8,7
&	8000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	12
!	4820	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	11,8,2
¡	40A0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	11,8,6
¬	4060	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	11,8,7
%	2220	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0,8,4
_	2120	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0,8,5
>	20A0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0,8,6
?	2060	0	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0,8,7
:	0820	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	8,2
#	0420	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	8,3
@	0220	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	8,4
"	0060	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	8,7
0-8-2	2820	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0,8,2

Area Codes

I/O Device	Area Code (Binary)	(Hex)
Console Operations	(00000)	0
1816/1053 Printers (first 4)	(00001)	1
1442 Card Read Punch (first)	(00010)	2
1054/1055 Paper Tape Units	(00011)	3
1810 Disk Storage (A1) (B1)	(00100)	4
1810 Disk Storage (A2) (B2)	(01000)	8
1810 Disk Storage (A3) (B3)	(01001)	9
1627 Plotter	(00101)	5
1443 Printer	(00110)	6
Analog Input	(01010)	A
Digital Input (Digital and Pulse Count)	(01011)	B
Digital and Analog Output (DO, ECO, RO, AO)	(01100)	C
System/360 Adapter	(01101)	D
2401/2402 Magnetic Tape Units	(01110)	E
1816/1053 Printers (second 4)	(01111)	F
1442 Card Read Punch (second)	(10001)	11
Analog Input Expander	(10000)	10

1053/1816 Printer Control Characters

Function	0 1 2 3 4 5 6 7 8 15	Hex
Carrier Return	1 0 0 0 0 0 0 1	81
Tabulate	0 1 0 0 0 0 0 1	41
Space	0 0 1 0 0 0 0 1	21
Backspace	0 0 0 1 0 0 0 1	11
Shift to Red	0 0 0 0 1 0 0 1	09
Shift to Black	0 0 0 0 0 1 0 1	05
Line Feed	0 0 0 0 0 0 1 1	03

2401/2402 Control Functions

Bit Positions 13	14	15	Control Function
0	0	0	Rewind and Unload
0	0	1	Write Tape Mark
0	1	0	Erase
0	1	1	Backspace
1	0	0	Rewind

1443 Character Coding

Char	Hex	Bits 0 8	1 9	2 10	3 11	4 12	5 13	6 14	7 15	Typebar Character Set 63	52	39	13
A	31	0	0	1	1	0	0	0	1	x	x	x	
B	32	0	0	1	1	0	0	1	0	x	x	x	
C	33	0	0	1	1	0	0	1	1	x	x	x	
D	34	0	0	1	1	0	1	0	0	x	x	x	
E	35	0	0	1	1	0	1	0	1	x	x	x	
F	36	0	0	1	1	0	1	1	0	x	x	x	
G	37	0	0	1	1	0	1	1	1	x	x	x	
H	38	0	0	1	1	1	0	0	0	x	x	x	
I	39	0	0	1	1	1	0	0	1	x	x	x	
J	21	0	0	1	0	0	0	0	1	x	x	x	
K	22	0	0	1	0	0	0	1	0	x	x	x	
L	23	0	0	1	0	0	0	1	1	x	x	x	
M	24	0	0	1	0	0	1	0	0	x	x	x	
N	25	0	0	1	0	0	1	0	1	x	x	x	
O	26	0	0	1	0	0	1	1	0	x	x	x	
P	27	0	0	1	0	0	1	1	1	x	x	x	
Q	28	0	0	1	0	1	0	0	0	x	x	x	
R	29	0	0	1	0	1	0	0	1	x	x	x	
S	12	0	0	0	1	0	0	1	0	x	x	x	
T	13	0	0	0	1	0	0	1	1	x	x	x	
U	14	0	0	0	1	0	1	0	0	x	x	x	
V	15	0	0	0	1	0	1	0	1	x	x	x	
W	16	0	0	0	1	0	1	1	0	x	x	x	
X	17	0	0	0	1	0	1	1	1	x	x	x	
Y	18	0	0	0	1	1	0	0	0	x	x	x	
Z	19	0	0	0	1	1	0	0	1	x	x	x	
1	01	0	0	0	0	0	0	0	1	x	x	x	x
2	02	0	0	0	0	0	0	1	0	x	x	x	x
3	03	0	0	0	0	0	0	1	1	x	x	x	x
4	04	0	0	0	0	0	1	0	0	x	x	x	x
5	05	0	0	0	0	0	1	0	1	x	x	x	x
6	06	0	0	0	0	0	1	1	0	x	x	x	x
7	07	0	0	0	0	0	1	1	1	x	x	x	x
8	08	0	0	0	0	1	0	0	0	x	x	x	x
9	09	0	0	0	0	1	0	0	1	x	x	x	x
0	0A	0	0	0	0	1	0	1	0	x	x	x	x
+	10	0	0	0	1	0	0	0	0	x	x		
&	30	0	0	1	1	0	0	0	0	x	x		
-	20	0	0	1	0	0	0	0	0	x	x		x
/	11	0	0	0	1	0	0	0	1	x	x		
%	1A	0	0	0	1	1	0	1	0	x	x		
¤	3A	0	0	1	1	1	0	1	0	x	x		
#	2A	0	0	1	0	1	0	1	0	x	x		
=	08	0	0	0	0	1	0	1	1	x	x		
,	1B	0	0	0	1	1	0	1	1	x	x	x	
.	3B	0	0	1	1	1	0	1	1	x	x	x	x
$	2B	0	0	1	0	1	0	1	1	x	x	x	
@	0C	0	0	0	0	1	1	0	0	x	x		
(	1C	0	0	0	1	1	1	0	0	x	x		
)	3C	0	0	1	1	1	1	0	0	x	x		
*	2C	0	0	1	0	1	1	0	0	x	x		x
'	0D	0	0	0	0	1	1	0	1	x	x		
¯	1D	0	0	0	1	1	1	0	1	x			
ç	3D	0	0	1	1	1	1	0	1	x			
		2D	0	0	1	0	1	1	0	1	x		
>	0E	0	0	0	0	1	1	1	0	x			
:	1E	0	0	0	1	1	1	1	0	x			
<	3E	0	0	1	1	1	1	1	0	x			
;	2E	0	0	1	0	1	1	1	0	x			
?	0F	0	0	0	0	1	1	1	1	x			
"	1F	0	0	0	1	1	1	1	1	x			
¦	3F	0	0	1	1	1	1	1	1	x			
¬	2F	0	0	1	0	1	1	1	1	x			

1443 Carriage Control Characters

Immediate Skip to	Hex	Bit 0 1 2 3 4 5 6 7	Skip after Print to	Hex	Bit 0 1 2 3 4 5 6 7
Channel 1	01	0 0 0 0 0 0 0 0 1	Channel 1	31	0 0 1 1 0 0 0 1
Channel 2	02	0 0 0 0 0 0 1 0	Channel 2	32	0 0 1 1 0 0 1 0
Channel 3	03	0 0 0 0 0 0 1 1	Channel 3	33	0 0 1 1 0 0 1 1
Channel 4	04	0 0 0 0 0 1 0 0	Channel 4	34	0 0 1 1 0 1 0 0
Channel 5	05	0 0 0 0 0 1 0 1	Channel 5	35	0 0 1 1 0 1 0 1
Channel 6	06	0 0 0 0 0 1 1 0	Channel 6	36	0 0 1 1 0 1 1 0
Channel 7	07	0 0 0 0 0 1 1 1	Channel 7	37	0 0 1 1 0 1 1 1
Channel 8	08	0 0 0 0 1 0 0 0	Channel 8	38	0 0 1 1 1 0 0 0
Channel 9	09	0 0 0 0 1 0 0 1	Channel 9	39	0 0 1 1 1 0 0 1
Channel 10	0A	0 0 0 0 1 0 1 0	Channel 10	3A	0 0 1 1 1 0 1 0
Channel 11	0B	0 0 0 0 1 0 1 1	Channel 11	3B	0 0 1 1 1 0 1 1
Channel 12	0C	0 0 0 0 1 1 0 0	Channel 12	3C	0 0 1 1 1 1 0 0
Immediate Space			Space after Print		
1 Space	21	0 0 1 0 0 0 0 1	1 Space	11	0 0 0 1 0 0 0 1
2 Spaces	22	0 0 1 0 0 0 1 0	2 Spaces	12	0 0 0 1 0 0 1 0
3 Spaces	23	0 0 1 0 0 0 1 1	3 Spaces	13	0 0 0 1 0 0 1 1

Instruction Set

Hexadecimal	Load and Store Instructions
	Load Accumulator (LD)
C0XX	Contents of CSL at EA (I+DISP) are loaded into A
C1XX	Contents of CSL at EA (XR1+DISP) are loaded into A
C2XX	Contents of CSL at EA (XR2+DISP) are loaded into A
C3XX	Contents of CSL at EA (XR3+DISP) are loaded into A
C400XXXX	Contents of CSL at EA (Addr) are loaded into A
C500XXXX	Contents of CSL at EA (Addr +XR1) are loaded into A
C600XXXX	Contents of CSL at EA (Addr +XR2) are loaded into A
C700XXXX	Contents of CSL at EA (Addr +XR3) are loaded into A
C480XXXX	Contents of CSL at EA (V in CSL at Addr) are loaded into A
C580XXXX	Contents of CSL at EA (V in CSL at "Addr +XR1") are loaded into A
C680XXXX	Contents of CSL at EA (V In CSL at "Addr +XR2") are loaded into A
C780XXXX	Contents of CSL at EA (V in CSL at "Addr +XR3") are loaded into A
	Double Load (LDD)
C8XX	Contents of CSL at EA (I + DISP) and EA+1 are loaded into A and Q
C9XX	Contents of CSL at EA(XR1 + DISP) and EA+1 are loaded into A and Q
CAXX	Contents of CSL at EA (XR2 + DISP) and EA+1 are loaded into A and Q
CBXX	Contents of CSL at EA (XR3 + DISP) and EA+1 are loaded into A and Q
CC00XXXX	Contents of CSL at EA (Addr) and EA+1 are loaded into A and Q
CD00XXXX	Contents of CSL at EA (Addr +XR1) and EA+1 are loaded into A and Q
CE00XXXX	Contents of CSL at EA (Addr +XR2) and EA+1 are loaded into A and Q
CF00XXXX	Contents of CSL at EA (Addr +XR3) and EA+1 are loaded into A and Q
CC80XXXX	Contents of CSL at EA (V in CSL at Addr) and EA+1 are loaded into A and Q
CD80XXXX	Contents of CSL at EA (V in CSL at "Addr +XR1") and EA+1 are loaded into A and Q
CE80XXXX	Contents of CSL at EA (V In CSL at "ADDR +XR2") and EA+1 are loaded into A and Q
CF80XXXX	Contents of CSL at EA (V in CSL at "Addr +XR3") and EA+1 are loaded into A and Q
	Store Accumulator (STO)
D0XX	Contents of A are stored in CSL at EA (I+DISP)
D1XX	Contents of A are stored in CSL at EA (XR1+DISP)
D2XX	Contents of A are stored in CSL at EA (XR2+DISP)
D3XX	Contents of A are stored in CSL at EA (XR3+DISP)
D400XXXX	Contents of A are stored in CSL at EA (Addr)
D500XXXX	Contents of A are stored in CSL at EA (Addr +XR1)
D600XXXX	Contents of A are stored in CSL at EA (Addr +XR2)
D700XXXX	Contents of A are stored in CSL at EA (Addr +XR3)
D480XXXX	Contents of A are stored In CSL at EA (V in CSL at Addr)
D580XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr +XR1")
D680XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr +XR2")
D780XXXX	Contents of A are stored in CSL at EA (V in CSL at "Addr +XR3")
	Double Store (STD)
D8XX	Contents of A and Q are stored in CSL at EA (I+DISP) and EA+1
D9XX	Contents of A and Q are stored in CSL at EA (XR1 +DISP) and EA+1
DAXX	Contents of A and Q are stored in CSL at EA (XR2 +DISP) and EA+1
DBXX	Contents of A and Q are stored in CSL at EA (XR3 +DISP) and EA+1
DC00XXXX	Contents of A and Q are stored in CSL at EA (Addr) and EA+1
DD00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR1) and EA+1
DE00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR2) and EA+1
DF00XXXX	Contents of A and Q are stored in CSL at EA (Addr +XR3) and EA+1
DC80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at Addr) and EA+1
DD80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR1") and EA+1
DE80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR2") and EA+1
DF80XXXX	Contents of A and Q are stored in CSL at EA (V in CSL at "Addr +XR3") and EA+1
	Load Index (LDX)
60XX	Load DISP into the Instruction Register
61XX	Load DISP into Index Register 1
62XX	Load DISP into Index Register 2
63XX	Load DISP into Index Register 3
6400XXXX	Load Addr into the Instruction Register
6500XXXX	Load Addr into Index Register 1
6600XXXX	Load Addr into Index Register 2
6700XXXX	Load Addr into Index Register 3
6480XXXX	Load contents of CSL at Addr into the Instruction Register
6580XXXX	Load contents of CSL at Addr into Index Register 1
6680XXXX	Load contents of CSL at Addr Into Index Register 2
6780XXXX	Load contents of CSL at Addr Into Index Register 3
	Store Index (STX)
68XX	Store I in CSL at EA (I+DISP)
69XX	Store XR1 in CSL at EA (I+DISP)
6AXX	Store XR2 in CSL at EA (I+DISP)
6BXX	Store XR3 in CSL at EA (I+DISP)
6C00XXXX	Store I in CSL at EA (Addr)
6D00XXXX	Store XR1 in CSL at EA (Addr)
6E00XXXX	Store XR2 in CSL at EA (Addr)
6F00XXXX	Store XR3 in CSL at EA (Addr)
6C80XXXX	Store I in CSL at EA (V in CSL at Addr)
6D80XXXX	Store XR1 in CSL at EA (V in CSL at Addr)
6E80XXXX	Store XR2 in CSL at EA (V in CSL at Addr)
6F80XXXX	Store XR3 in CSL at EA (V in CSL at Addr)
	Store Status (STS)
28XX	Store status of Indicators in CSL at EA (I+DISP)
29XX	Store status of Indicators in CSL at EA (XR1+DISP)
2AXX	Store status of Indicators in CSL at EA (XR2+DISP)
2BXX	Store status of indicators in CSL at EA (XR3+DISP)
2C00XXXX	Store status of indicators in CSL at EA (Addr)

Hexadecimal	Load and Store Instructions
2D00XXXX	Store status of indicators in CSL at EA (Addr+XR1)
2E00XXXX	Store status of indicators in CSL at EA (Addr+XR2)
2F00XXXX	Store status of indicators in CSL at EA (Addr+XR3)
2C80XXXX	Store status of indicators in CSL at EA (V in CSL at Addr)
2D80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr +XR1")
2E80XXXX	Store status of Indicators in CSL at EA (V in CSL at "Addr +XR2")
2F80XXXX	Store status of indicators in CSL at EA (V in CSL at "Addr +XR3")
2C40XXXX	Clear storage protect bit in CSL at EA (Addr)
2C41XXXX	Write storage protect bit in CSL at EA (Addr)
2D40XXXX	Clear storage protect bit in CSL at EA (Addr +XR1)
2D41XXXX	Write storage protect bit in CSL at EA (Addr +XR1)
2E40XXXX	Clear storage protect bit in CSL at EA (Addr +XR2)
2E41XXXX	Write storage protect bit in CSL at EA (Addr +XR2)
2F40XXXX	Clear storage protect bit in CSL at EA (Addr +XR3)
2F41XXXX	Write storage protect bit in CSL at EA (Addr +XR3)
2CC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at Addr)
2CC1XXXX	Write storage protect bit in CSL at EA (V in CSL at Addr)
2DC0XXXX	Clear storage protect bit In CSL at EA (V in CSL at "Addr +XR1")
2DC1XXXX	Write storage protect bit In CSL at EA (V in CSL at "Addr +XR1")
2EC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR2")
2EC1XXXX	Write storage protect bit in CSL at EA (V in CSL at "Addr +XR2")
2FC0XXXX	Clear storage protect bit in CSL at EA (V in CSL at "Addr +XR3")
2FC1XXXX	Write storage protect bit In CSL at EA (V in CSL at "Addr +XR3")
	Load Status (LDS)
2000	Set CARRY and OVERFLOW indicators OFF
2001	Set OVERFLOW ON and CARRY OFF
2002	Set OVERFLOW OFF and CARRY ON
2003	Set CARRY and OVERFLOW indicator ON
	Arithmetic Instructions
	Add (A)
80XX	Add contents of CSL at EA (I+DISP) to A
81XX	Add contents of CSL at EA (XR1+DISP) to A
82XX	Add contents of CSL at EA (XR2+DISP) to A
83XX	Add contents of CSL at EA (XR3+DISP) to A
8400XXXX	Add contents of CSL at EA (Addr) to A
8500XXXX	Add contents of CSL at EA (Addr +XR1) to A
8600XXXX	Add contents of CSL at EA (Addr +XR2) to A
8700XXXX	Add contents of CSL at EA (Addr +XR3) to A
8480XXXX	Add contents of CSL at EA (V in CSL at Addr) to A
8580XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR1") to A
8680XXXX	Add contents of CSL at EA (V In CSL at "Addr+XR2") to A
8780XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR3") to A
	Double Add (AD)
88XX	Add contents of CSL at EA (I+DISP) and EA+1 to A and Q
89XX	Add contents of CSL at EA (XR1+DISP) and EA+1 to A and Q
8AXX	Add contents of CSL at EA (XR2+DISP) and EA+1 to A and Q
8BXX	Add contents of CSL at EA (XR3+DISP) and EA+1 to A and Q
8C00XXXX	Add contents of CSL at EA (Addr) and EA+1 to A and Q
8D00XXXX	Add contents of CSL at EA (Addr+XR1) and EA+1 to A and Q
8E00XXXX	Add contents of CSL at EA (Addr+XR2) and EA+1 to A and Q
8F00XXXX	Add contents of CSL at EA (Addr+XR3) and EA+1 to A and Q
8C80XXXX	Add contents of CSL at EA (V in CSL at Addr) and EA+1 to A and Q
8D80XXXX	Add contents of CSL at EA (V In CSL at "Addr+XR1") and EA+1 to A and Q
8E80XXXX	Add contents of CSL at EA (V in CSL at "Addr+XR2") and EA+1 to A and Q
8F80XXXX	Add contents of CSL at EA(V in CSL at "Addr+XR3")and EA+1 to A and Q
	Subtract (S)
90XX	Subtract contents of CSL at EA (I+DISP) from A
91XX	Subtract contents of CSL at EA (XR1+DISP) from A
92XX	Subtract contents of CSL at EA (XR2+DISP) from A
93XX	Subtract contents of CSL at EA (XR3+DISP) from A
9400XXXX	Subtract contents of CSL at EA (Addr) from A
9500XXXX	Subtract contents of CSL at EA (Addr+XR1) from A
9600XXXX	Subtract contents of CSL at EA (Addr+XR2) from A
9700XXXX	Subtract contents of CSL at EA (Addr+XR3) from A
9480XXXX	Subtract contents of CSL at EA (V In CSL at Addr) from A
9580XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") from A
9680XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR2") from A
9780XXXX	Subtract contents of CSL at EA (V In CSL at "Addr+XR3") from A
	Double Subtract (SD)
98XX	Subtract contents of CSL at EA (I+DISP) and EA+1 from A and Q
99XX	Subtract contents of CSL at EA (XR1+DISP) and EA+1 from A and Q
9AXX	Subtract contents of CSL at EA (XR2+DISP) and EA+1 from A and Q
9BXX	Subtract contents of CSL at EA (XR3+DISP) and EA+1 from A and Q
9C00XXXX	Subtract contents of CSL at EA (Addr) and EA+1 from A and Q
9D00XXXX	Subtract contents of CSL at EA (Addr+XR1) and EA+1 from A and Q
9E00XXXX	Subtract contents of CSL at EA (Addr+XR2) and EA+1 from A and Q
9F00XXXX	Subtract contents of CSL at EA (Addr+XR3) and EA+1 from A and Q
9C80XXXX	Subtract contents of CSL at EA (V In CSL at Addr) and EA+1 from A and Q
9D80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR1") and EA+1 from A and Q
9E80XXXX	Subtract contents of CSL at EA (V In CSL at "Addr+XR2") and EA+1 from A and Q
9F80XXXX	Subtract contents of CSL at EA (V in CSL at "Addr+XR3") and EA+1 from A and Q
	Multiply (M)
A0XX	Multiply contents of CSL at EA (I+DISP) by A
A1XX	Multiply contents of CSL at EA (XR1+DISP) by A
A2XX	Multiply contents of CSL at EA (XR2+DISP) by A
A3XX	Multiply contents of CSL at EA (XR3+DISP) by A
A400XXXX	Multiply contents of CSL at EA (Addr) by A

Instruction Set

Hexadecimal	Arithmetic Instructions
A500XXXX	Multiply contents of CSL at EA (Addr+XR1) by A
A600XXXX	Multiply contents of CSL at EA (Addr+XR2) by A
A700XXXX	Multiply contents of CSL at EA (Addr+XR3) by A
A480XXXX	Multiply contents of CSL at EA (V in CSL at Addr) by A
A580XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR1") by A
A680XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR2") by A
A780XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR3") by A
	Divide (D)
A8XX	Divide A and Q by contents of CSL at EA (I+DISP)
A9XX	Divide A and Q by contents of CSL at EA (XR1+DISP)
AAXX	Divide A and Q by contents of CSL at EA (XR2+DISP)
ABXX	Divide A and Q by contents of CSL at EA (XR3+DISP)
AC00XXXX	Divide A and Q by contents of CSL at EA (Addr)
AD00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR1)
AE00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR2)
AF00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR3)
AC80XXXX	Divide A and Q by contents of CSL at EA(V in CSL at Addr)
AD80XXXX	Divide A and Q by contents of CSL at EA(V in CSL at "Addr+XR1"
AE80XXXX	Divide A and Q by contents of CSL at EA(V in CSL at "Addr+XR2"
AF80XXXX	Divide A and Q by contents of CSL at EA(V in CSL at "Addr+XR3"
	Logical And (AND)
E0XX	AND contents of CSL at EA (I+DISP) with A
E1XX	AND contents of CSL at EA (XR1+DISP) with A
E2XX	AND contents of CSL at EA (XR2+DISP) with A
E3XX	AND contents of CSL at EA (XR3+DISP) with A
E400XXXX	AND contents of CSL at EA (Addr) with A
E500XXXX	AND contents of CSL at EA (Addr+XR1) with A
E600XXXX	AND contents of CSL at EA (Addr+XR2) with A
E700XXXX	AND contents of CSL at EA (Addr+XR3) with A
E480XXXX	AND contents of CSL at EA (V in CSL at Addr) with A
E580XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR1") with A
E680XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR2") with A
E780XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Logical Or (OR)
E8XX	OR contents of CSL at EA (I+DISP) with A
E9XX	OR contents of CSL at EA (XR1+DISP) with A
EAXX	OR contents of CSL at EA (XR2+DISP) with A
EBXX	OR contents of CSL at EA (XR3+DISP) with A
EC00XXXX	OR contents of CSL at EA (Addr) with A
ED00XXXX	OR contents of CSL at EA (Addr+XR1) with A
EE00XXXX	OR contents of CSL at EA (Addr+XR2) with A
EF00XXXX	OR contents of CSL at EA (Addr+XR3) with A
EC80XXXX	OR contents of CSL at EA (V in CSL at Addr) with A
ED80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR1") with A
EE80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR2") with A
EF80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Logical Exclusive Or (EOR)
F0XX	EOR contents of CSL at EA (I+DISP) with A
F1XX	EOR contents of CSL at EA (XR1+DISP) with A
F2XX	EOR contents of CSL at EA (XR2+DISP) with A
F3XX	EOR contents of CSL at EA (XR3+DISP) with A
F400XXXX	EOR contents of CSL at EA (Addr) with A
F500XXXX	EOR contents of CSL at EA (Addr+XR1) with A
F600XXXX	EOR contents of CSL at EA (Addr+XR2) with A
F700XXXX	EOR contents of CSL at EA (Addr+XR3) with A
F480XXXX	EOR contents of CSL at EA (V in CSL at Addr) with A
F580XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR1") with A
F680XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR2") with A
F780XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Shift Instructions
	Shift Left Logical A (SLA)
10*X	Contents of A shift left the number of shift counts in DISP
1100	Contents of A shift left the number of shift counts in XR1
1200	Contents of A shift left the number of shift counts in XR2
1300	Contents of A shift left the number of shift counts in XR3
	Shift Left Logical A & Q (SLT)
10*X	Contents of A and Q shift left the number of shift counts In DISP
1180	Contents of A and Q shift left the number of shift counts in XR1
1280	Contents of A and Q shift left the number of shift counts in XR2
1380	Contents of A and Q shift left the number of shift counts In XR3
	Shift Left And Count A (SLCA)
10*X	Contents of A shift left the number of shift counts in DISP
1140	Contents of A shift left the number of shift counts in XR1
1240	Contents of A shift left the number of shift counts in XR2
1340	Contents of A shift left the number of shift counts in XR3
	Shift Left And Count A & Q (SLC)
10*X	Contents of A and Q shift left the number of shift counts in DISP
11C0	Contents of A and Q shift left the number of shift counts in XR1
12C0	Contents of A and Q shift left the number of shift counts In XR2
13C0	Contents of A and Q shift left the number of shift counts in XR3
	Shift Right Logical A (SRA)
18*X	Contents of A shift right the number of shift counts In DISP
1900	Contents of A shift right the number of shift counts in XR1
1A00	Contents of A shift right the number of shift counts in XR2
1B00	Contents of A shift right the number of shift counts in XR3

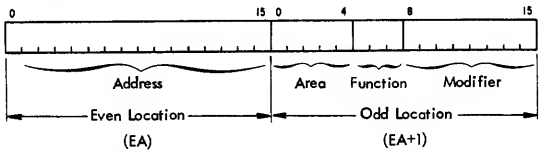
Hexadecimal	Shift Instructions
	Shift Right A & Q (SRT)
18*X	Contents of A and Q shift right the number of shift counts in DISP
1980	Contents of A and Q shift right the number of shift counts in XR1
1A80	Contents of A and Q shift right the number of shift counts in XR2
1B80	Contents of A and Q shift right the number of shift counts in XR3
	Rotate Right A & Q (RTE)
18*X	Contents of A and Q rotate right the number of counts in DISP
19C0	Contents of A and Q rotate right the number of counts in XR1
1AC0	Contents of A and Q rotate right the number of counts in XR2
1BC0	Contents of A and Q rotate right the number of counts in XR3
	Branch Instructions
	Branch Or Skip On Condition (BSC or BOSC)
48*X	Skip the next one-word instruction if ANY condition is sensed
4C*XXXXX	Branch to CSL at EA (Addr) on NO condition
4D*XXXXX	Branch to CSL at EA (Addr+XR1) on NO condition
4E*XXXXX	Branch to CSL at EA (Addr+XR2) on NO condition
4F*XXXXX	Branch to CSL at EA (Addr+XR3) on NO condition
4C*XXXXX	Branch to CSL at EA (V in CSL at Addr) on NO condition
4D*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR1") on NO condition
4E*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR2") on NO condition
4F*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR3") on NO condition
	Branch And Store Instruction Register (BSI)
40XX	Store next sequential address in CSL at EA (I+DISP) and Branch to EA+1
41XX	Store next sequential address in CSL at EA (XR1+DISP) and Branch to EA+1
42XX	Store next sequential address in CSL at EA (XR2+DISP) and Branch to EA+1
43XX	Store next sequential address in CSL at EA (XR3+DISP) and Branch to EA+1
44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR1) and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR2) and Branch to EA+1
47*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR3) and Branch to EA+1
44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR1") and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR2") and Branch to EA+1
47*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V In CSL at "Addr+XR3") and Branch to EA+1
	Modify Index and Skip (MDX)
70XX	ADD expanded DISP to I (no skip con occur)
71XX	ADD expanded DISP to XR1
72XX	ADD expanded DISP to XR2
73XX	ADD expanded DISP to XR3
74XXXXXX	Add expanded positive DISP to CSL at Addr (Add to memory)
7500XXXX	Add Addr to XR1
7600XXXX	Add Addr to XR2
7700XXXX	Add Addr to XR3
74XXXXXX	Add expanded negative DISP to CSL at Addr (Add to Memary)
7580XXXX	Add V in CSL at Addr to XR1
7680XXXX	Add V in CSL at Addr to XR2
7780XXXX	Add V in CSL at Addr to XR3
	Wait (WAIT)
3000	WAIT until monual start or until completion of an interrupt subroutine
	Compare (CMP)
B0XX	Compare A with contents of CSL at EA (I+DISP)
B1XX	Compare A with contents of CSL at EA (XR1+DISP)
B2XX	Compare A with contents of CSL at EA (XR2+DISP)
B3XX	Compare A with contents of CSL at EA (XR3+DISP)
B400XXXX	Compare A with contents of CSL at EA (Addr)
B500XXXX	Compare A with contents of CSL at EA (Addr+XR1)
B600XXXX	Compare A with contents of CSL at EA (Addr+XR2)
B700XXXX	Compare A with contents of CSL at EA (Addr+XR3)
B480XXXX	Compare A with contents of CSL at EA (V in CSL at Addr)
B580XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR1")
B680XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR2")
B780XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR3")
	Double Compare (DCM)
B8XX	Compare A and Q with contents of CSL at EA (I+DISP) and EA+1
B9XX	Compare A and Q with contents of CSL at EA (XR1+DISP) and EA+1
BAXX	Compare A and Q with contents of CSL at EA (XR2+DISP) and EA+1
BBXX	Compare A and Q with contents of CSL at EA (XR3+DISP) and EA+1
BC00XXXX	Compare A and Q with contents of CSL at EA (Addr) and EA+1
BD00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR1) and EA+1

Input/Output Control Commands

Device/Function	IOCC: Address Word (Hex.)	Area, Function, and Modifier Word (Hex.)		
Console (Area 00000) Continued				
Interrupt (Console) Sense	0000	Load Indicator Status to A-register	07C0 1	-Reset Indicator
Operations Monitor Control	0000	Reset Timer	04E1	
Interval Timers Sense	0000	Load Indicator Status to A-register	0720 1	-Reset Indicator
Control	X000 0 1 2 3 Timer A B C 0 1 = Start Timer 0 = Stop Timer	Start or Stop Timer	0420	
Interrupt Mask Register Control	XXXX (Levels 0-13 use bits 0-13, Levels 14-23 use bits 0-9) 1-bit = mask 0-bit = unmask	Levels 0-13- Levels 14-23-	0480 0481	
Program Interrupt Control	XXXX (Generate Interrupt with 1-bit. Levels 0-13 use bits 0-13, Levels 14-23 use bits 0-9.)	Levels 0-13- Levels 14-23-	04A0 04A1	
Digital Input				
Direct Program Control Read	XXXX (Addr to Store Digit Input Group)	DI or PI Group to Core Storage	5A XX	-DI Addr 40 thru 7F or PI Addr 02 thru 19
Sense Device	0000	DSW, DI, or PISW A-register	5F 00 01 XX	-DSW -DSW, Reset Indicators -DI Addr 40 thru 7F or PISW Addr 02 thru 19
Control	0000	Generate Reset to DI Controls	5C20	
Data Channel Control Initialize Read	XXXX (Addr of Data Table)	Set up DC Controls for Transfer of Data	5E X0 8 9 10 11 [0] 00 = Read Random 01 = Read Sequential 10 = Read Single 1 = Ex. Sync.	
Analog Input				
Direct Program Control Write	XXXX (Mpx Addr Location)	AI- AIE-	51 81 XX 8 9 10 11 12 13 14 15 [00 000] 00 = 11-bit res. 01 = 14-bit res. 10 = 8-bit res. 1 = Ex. Sync.	Analog Input to ADC
Read	XXXX (Addr to Store ADC Reading)	AI- AIE-	52 82 00 80 -Sequential Programmed Operation	ADC to Core
Control	0000	AI- AIE-	5400 8400	Reset Controls and Registers
Sense Device	0000	AI- AIE-	57 87 0 8 1	-AI -Comparator -Reset Indicators

Device/Function	IOCC: Address Word (Hex.)	Area, Function, and Modifier Word (Hex.)		
Analog Input Continued				
Data Channel Control Initialize Write	XXXX (First Mpx Addr Table Location)	AI- AIE-	5500 8500	(Set up DC for Transfer of Mpx Addr and Limit Words)
Initialize Read	XXXX (First Data Toble Addr)	AI- AIE-	56 86 XX 8 9 10 11 12 13 14 15 [0 000] 00 = 11-bit res. 01 = 14-bit res. 10 = 8 - bit res. 0 = 1 DC Operation 1 = 2 DC Operation 1 = Ex. Sync.	
Digital and Analog Output				
Direct Program Control Write	XXXX (Addr of Output Data)	Core Storage to DAO Device	61 XX	-DAO Register Addr 00 thru 7F
Control	0000		64 20 40 80	-Reset DAO Controls -Initiate Simultaneous Transfer from Registers -Start Pulse Output Timer
Sense Device	0000	DSW to A A-register	6700 01	-Reset Indicators
Data Channel Control Initialize Write	XXXX (Addr of Data Table)	Set up DC Controls to Transfer Data	65 X0 8 9 10 11 [0 0] 0 = Random 1 = Single 1 = Ex. Sync.	

IOCC Format



Interrupts

Interrupt	Priority Level	Core Storage Location Decimal	Core Storage Location Hex.	ILSW	
Internal	1	8	8	Yes	
Trace	26	9	9	No	
** CE	27	10	A	No	
*External 0	2	11	B	Yes	
1	3	12	C	Yes	
2	4	13	D	Yes	
3	5	14	E	Yes	
4	6	15	F	Yes	Basic
5	7	16	10	Yes	
6	8	17	11	Yes	
7	9	18	12	Yes	
8	10	19	13	Yes	
9	11	20	14	Yes	
10	12	21	15	Yes	
11	13	22	16	Yes	
12	14	23	17	Yes	
13	15	24	18	Yes	
14	16	25	19	Yes	Special Feature Group 1
15	17	26	1A	Yes	
16	18	27	1B	Yes	
17	19	28	1C	Yes	
18	20	29	1D	Yes	
19	21	30	1E	Yes	Special Feature Group 2
20	22	31	1F	Yes	
21	23	32	20	Yes	
22	24	33	21	Yes	
23	25	34	22	Yes	

* External interrupt cannot occur at the end of an XIO or BSI instruction.

** A CE interrupt Stores the return link in core location 10 (decimal) and starts execution at core location 0001. Interrupts are prevented in the same manner as for the standard forced BSI.

Instruction Set

Hexadecimal	Arithmetic Instructions
A500XXXX	Multiply contents of CSL at EA (Addr+XR1) by A
A600XXXX	Multiply contents of CSL at EA (Addr+XR2) by A
A700XXXX	Multiply contents of CSL at EA (Addr+XR3) by A
A480XXXX	Multiply contents of CSL at EA (V in CSL at Addr) by A
A580XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR1") by A
A680XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR2") by A
A780XXXX	Multiply contents of CSL at EA (V in CSL at "Addr+XR3") by A
	Divide (D)
A8XX	Divide A and Q by contents of CSL at EA (I+DISP)
A9XX	Divide A and Q by contents of CSL at EA (XR1+DISP)
AAXX	Divide A and Q by contents of CSL at EA (XR2+DISP)
ABXX	Divide A and Q by contents of CSL at EA (XR3+DISP)
AC00XXXX	Divide A and Q by contents of CSL at EA (Addr)
AD00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR1)
AE00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR2)
AF00XXXX	Divide A and Q by contents of CSL at EA (Addr+XR3)
AC80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at Addr)
AD80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR1"
AE80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR2"
AF80XXXX	Divide A and Q by contents of CSL at EA (V in CSL at "Addr+XR3"
	Logical And (AND)
E0XX	AND contents of CSL at EA (I+DISP) with A
E1XX	AND contents of CSL at EA (XR1+DISP) with A
E2XX	AND contents of CSL at EA (XR2+DISP) with A
E3XX	AND contents of CSL at EA (XR3+DISP) with A
E400XXXX	AND contents of CSL at EA (Addr) with A
E500XXXX	AND contents of CSL at EA (Addr+XR1) with A
E600XXXX	AND contents of CSL at EA (Addr+XR2) with A
E700XXXX	AND contents of CSL at EA (Addr+XR3) with A
E480XXXX	AND contents of CSL at EA (V in CSL at Addr) with A
E580XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR1") with A
E680XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR2") with A
E780XXXX	AND contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Logical Or (OR)
E8XX	OR contents of CSL at EA (I+DISP) with A
E9XX	OR contents of CSL at EA (XR1+DISP) with A
EAXX	OR contents of CSL at EA (XR2+DISP) with A
EBXX	OR contents of CSL at EA (XR3+DISP) with A
EC00XXXX	OR contents of CSL at EA (Addr) with A
ED00XXXX	OR contents of CSL at EA (Addr+XR1) with A
EE00XXXX	OR contents of CSL at EA (Addr+XR2) with A
EF00XXXX	OR contents of CSL at EA (Addr+XR3) with A
EC80XXXX	OR contents of CSL at EA (V in CSL at Addr) with A
ED80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR1") with A
EE80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR2") with A
EF80XXXX	OR contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Logical Exclusive Or (EOR)
F0XX	EOR contents of CSL at EA (I+DISP) with A
F1XX	EOR contents of CSL at EA (XR1+DISP) with A
F2XX	EOR contents of CSL at EA (XR2+DISP) with A
F3XX	EOR contents of CSL at EA (XR3+DISP) with A
F400XXXX	EOR contents of CSL at EA (Addr) with A
F500XXXX	EOR contents of CSL at EA (Addr+XR1) with A
F600XXXX	EOR contents of CSL at EA (Addr+XR2) with A
F700XXXX	EOR contents of CSL at EA (Addr+XR3) with A
F480XXXX	EOR contents of CSL at EA (V in CSL at Addr) with A
F580XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR1") with A
F680XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR2") with A
F780XXXX	EOR contents of CSL at EA (V in CSL at "Addr+XR3") with A
	Shift Instructions
	Shift Left Logical A (SLA)
10*X	Contents of A shift left the number of shift counts in DISP
1100	Contents of A shift left the number of shift counts in XR1
1200	Contents of A shift left the number of shift counts in XR2
1300	Contents of A shift left the number of shift counts in XR3
	Shift Left Logical A & Q (SLT)
10*X	Contents of A and Q shift left the number of shift counts in DISP
1180	Contents of A and Q shift left the number of shift counts in XR1
1280	Contents of A and Q shift left the number of shift counts in XR2
1380	Contents of A and Q shift left the number of shift counts in XR3
	Shift Left And Count A (SLCA)
10*X	Contents of A shift left the number of shift counts in DISP
1140	Contents of A shift left the number of shift counts in XR1
1240	Contents of A shift left the number of shift counts in XR2
1340	Contents of A shift left the number of shift counts in XR3
	Shift Left And Count A & Q (SLC)
10*X	Contents of A and Q shift left the number of shift counts in DISP
11C0	Contents of A and Q shift left the number of shift counts in XR1
12C0	Contents of A and Q shift left the number of shift counts in XR2
13C0	Contents of A and Q shift left the number of shift counts in XR3
	Shift Right Logical A (SRA)
18*X	Contents of A shift right the number of shift counts in DISP
1900	Contents of A shift right the number of shift counts in XR1
1A00	Contents of A shift right the number of shift counts in XR2
1B00	Contents of A shift right the number of shift counts in XR3

Hexadecimal	Shift Instructions
	Shift Right A & Q (SRT)
18*X	Contents of A and Q shift right the number of shift counts in DISP
1980	Contents of A and Q shift right the number of shift counts in XR1
1A80	Contents of A and Q shift right the number of shift counts in XR2
1B80	Contents of A and Q shift right the number of shift counts in XR3
	Rotate Right A & Q (RTE)
18*X	Contents of A and Q rotate right the number of counts in DISP
19C0	Contents of A and Q rotate right the number of counts in XR1
1AC0	Contents of A and Q rotate right the number of counts in XR2
1BC0	Contents of A and Q rotate right the number of counts in XR3
	Branch Instructions
	Branch Or Skip On Condition (BSC or BOSC)
48*X	Skip the next one-word instruction if ANY condition is sensed
4C*XXXXX	Branch to CSL at EA (Addr) on NO condition
4D*XXXXX	Branch to CSL at EA (Addr+XR1) on NO condition
4E*XXXXX	Branch to CSL at EA (Addr+XR2) on NO condition
4F*XXXXX	Branch to CSL at EA (Addr+XR3) on NO condition
4C*XXXXX	Branch to CSL at EA (V in CSL at Addr) on NO condition
4D*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR1") on NO condition
4E*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR2") on NO condition
4F*XXXXX	Branch to CSL at EA (V in CSL at "Addr+XR3") on NO condition
	Branch And Store Instruction Register (BSI)
40XX	Store next sequential address in CSL at EA (I+DISP) and Branch to EA+1
41XX	Store next sequential address in CSL at EA (XR1+DISP) and Branch to EA+1
42XX	Store next sequential address in CSL at EA (XR2+DISP) and Branch to EA+1
43XX	Store next sequential address in CSL at EA (XR3+DISP) and Branch to EA+1
44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr) and Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR1) and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (Addr+XR2) and Branch to EA+1
47*XXXXX	If NO condition is true, store nextsequential address in CSL at EA (Addr+XR3) and Branch to EA+1
44*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at Addr) ond Branch to EA+1
45*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR1") and Branch to EA+1
46*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR2") and Branch to EA+1
47*XXXXX	If NO condition is true, store next sequential address in CSL at EA (V in CSL at "Addr+XR3") and Branch to EA+1
	Modify Index and Skip (MDX)
70XX	ADD expanded DISP to I (no skip can occur)
71XX	ADD expanded DISP to XR1
72XX	ADD expanded DISP to XR2
73XX	ADD expanded DISP to XR3
74XXXXXX	Add expanded positive DISP to CSL at Addr (Add to memory)
7500XXXX	Add Addr to XR1
7600XXXX	Add Addr to XR2
7700XXXX	Add Addr to XR3
74XXXXXX	Add expanded negative DISP to CSL at Addr (Add to Memory)
7580XXXX	Add V in CSL at Addr to XR1
7680XXXX	Add V in CSL at Addr to XR2
7780XXXX	Add V in CSL at Addr to XR3
	Wait (WAIT)
3000	WAIT until manual start or until completion of an interrupt subroutine
	Compare (CMP)
B0XX	Compare A with contents of CSL at EA (I+DISP)
B1XX	Compare A with contents of CSL at EA (XR1+DISP)
B2XX	Compare A with contents of CSL at EA (XR2+DISP)
B3XX	Compare A with contents of CSL at EA (XR3+DISP)
B400XXXX	Compare A with contents of CSL at EA (Addr)
B500XXXX	Compare A with contents of CSL at EA (Addr+XR1)
B600XXXX	Compare A with contents of CSL at EA (Addr+XR2)
B700XXXX	Compare A with contents of CSL at EA (Addr+XR3)
B480XXXX	Compare A with contents of CSL at EA (V in CSL at Addr)
B580XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR1")
B680XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR2")
B780XXXX	Compare A with contents of CSL at EA (V in CSL at "Addr+XR3")
	Double Compare (DCM)
B8XX	Compare A and Q with contents of CSL at EA (I+DISP) and EA+1
B9XX	Compare A and Q with contents of CSL at EA (XR1+DISP) and EA+1
BAXX	Compare A and Q with contents of CSL at EA (XR2+DISP) and EA+1
BBXX	Compare A and Q with contents of CSL at EA (XR3+DISP) and EA+1
BC00XXXX	Compare A and Q with contents of CSL at EA (Addr) and EA+1
BD00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR1) and EA+1

Input/Output Control Commands

Device/Function	IOCC		
	Address Word	Area, Function, and Modifier Word	
	Hex.	Hex.	
1816/1053			
Write	XXXX (Core Storage Addr)	1st-4th Printers- 09 5th-8th Printers- 79	
		02	-1st or 5th Printer
		04	-2nd or 6th Printer
		08	-3rd or 7th Printer
		10	-4th or 8th Printer
Sense Device	0000	1st-4th Printers- 0F 5th-8th Printers- 7F	
		02	-1st or 5th (03 if reset)
		04	-2nd or 6th (05 if reset)
		08	-3rd or 7th (09 if reset)
		10	-4th or 8th (11 if reset)
1816			
Read	XXXX (Core Storage Addr)	1st 1816- 0B02 2nd 1816- 7A02	Enter Input Character from Keyboard
Control	0000	1st 1816- 0C02 2nd 1816- 7C02	Place Keyboard in Proceed Status
1054/1055			
Read	XXXX (Core Storage Addr)	Read to Core- 1A00	
Write	XXXX (Core Storage Addr)	Punch from Core- 1900	
Control	0000	Read to Buffer- 1C10	-Initiate Reader Service Response Interrupt
Sense Device	0000	1054/1055- 1E00	
		01	-Reset Indicators
1442			
Initialize Read	XXXX (Table Addr)	1st 1442- 16 2nd 1442- 8D	
		00	-Card Image
		01	-Packed Mode
Initialize Write	XXXX (Table Addr)	1st 1442- 1500 2nd 1442- 8D00	Punch Core Image to Card Columns
Control	0000	1st 1442- 14 2nd 1442- 8C	
		02	-Feed Cycle
		80	-Stacker Select
		82	-Feed Cycle & Stacker Select
Sense Device	0000	1st 1442- 1700 2nd 1442- 8F00	
		01	-Reset Indicators
1443			
Initialize Write	XXXX (Table Addr)	3500	
		01	-Suppress Space After Print
Control	XX00 (Carriage Control Character)	Carriage Control- 3400	
Sense Device	0000	1443- 3700	
		01	-Reset Indicators
1627			
Write	XXXX (Core Storage Addr)	1627- 2900	
Sense Device	0000	1627- 2F00	
		01	-Reset Indicators
1810			
Control "A" Models	00XX (Number of Cylinder Movements)	1st drive- 24 2nd drive- 44 3rd drive- 4C	
		00	-Carriage Forward
		04	-Carriage Backward
Control "B" Models	00XX (Cylinder Addr)	1st drive- 24 2nd drive- 44 3rd drive- 4C	
		00	-Seek Specified Addr
		01	-Restore to Home Position
Initialize Read (A or B Model)	XXXX (Table Addr)	1st drive- 26 2nd drive- 46 3rd drive- 4E	
		0	-Read into Core
		8	-Read Check
		X	-Disk Sector

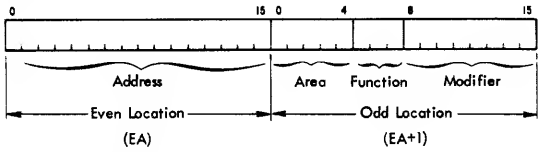
Device/Function	IOCC		
	Address Word	Area, Function, and Modifier Word	
	Hex.	Hex.	
1810 (Continued)			
Initialize Write (A or B Model)	XXXX (Table Addr)	1st drive- 25 2nd drive- 45 3rd drive- 4D	
		0X	-Disk Sector
Sense Device (A or B Model)	0000	1st drive- 2700 2nd drive- 4700 3rd drive- 4F00	
		01	-Reset Indicators
2401/2402			
Initialize Read	XXXX (Table Addr)	Tape to Core- 76XX	
		8 9 10 11 12 13 14 15	
		0 0	
		Parity*-0 = Odd, 1 = Even	
		1 = Rd-while-correcting	
		1 = Packed Format*	
		Density* 00 = 800 bpi, 01 = 200 bpi, 10 = SS6 bpi	
		0 = Tape Unit 0, 1 = Tape Unit 1	
		*Ignored on 9-Track	
Initialize Write	XXXX (Table Addr)	Core to Tape- 75XX	
		See Initialize Read (Bit 14 is not used)	
Control	0000	Control- 74XX	
		8 9 10 11 12 13 14 15	
		0 0	
		000 = Rewind Unload	
		001 = Write Tape Mark	
		010 = Erase	
		011 = Backspace	
		100 = Rewind	
		Density 00 = 800 bpi, 01 = 200 bpi, 10 = SS6 bpi	
		0 = Tape Unit 0, 1 = Tape Unit 1	
Sense Device	0000	77XX	
		8 9 10 11 12 13 14 15	
		0 0 , 0 0	
		1 = Reset Indicators	
		1 = Operation Stop	
		0 = Sense DSW	
		1 = Channel Word Count	
		0 = Select Tape Unit 0	
		1 = Select Tape Unit 1	
System/360 Adapter			
Initialize Write	XXXX (Table Addr)	Load Control Word to Adapter Buffer	6D00
Initialize Read	XXXX (Table Addr)	Load Control Word to Adapter Buffer	6E00
Sense Status	0000	Sense DSW-	6F00
		1	-Reset Indicators
Word Count	0000	Present Word Count of Data Channel	6F80
Control (Reset)	0000	Generate Reset to Adapter Controls	6C00
Console (Area 00000)			
Data Entry Switches Sense	0000	Load Content of Switches to A-register	0740
Read	XXXX (Core Storage Addr)	A-register to Core Storage	0240
Program Switches Sense	0000	Load Content of Switches to A-register	0760
Read	XXXX (Core Storoge Addr)	A-register to Core Storoge	0260

Input/Output Control Commands

Device/Function	IOCC: Address Word (Hex.)	IOCC: Area, Function, and Modifier Word		
Console (Area 00000) Continued				
Interrupt (Console) Sense	0000	Load Indicator Status to A-register	07C0 1	-Reset Indicator
Operations Monitor Control	0000	Reset Timer	04E1	
Interval Timers Sense	0000	Load Indicator Status to A-register	0720 1	-Reset Indicator
Control	X000 0 1 2 3 Timer: A 8 C 0 1 = Start Timer 0 = Stop Timer	Start or Stop Timer	0420	
Interrupt Mask Register Control	XXXX (Levels 0-13 use bits 0-13, Levels 14-23 use bits 0-9) 1-bit = mask 0-bit = unmask	Levels 0-13- Levels 14-23-	0480 0481	
Program Interrupt Control	XXXX (Generate Interrupt with 1-bit. Levels 0-13 use bits 0-13, Levels 14-23 use bits 0-9.)	Levels 0-13- Levels 14-23-	04A0 04A1	
Digital Input				
Direct Program Control Read	XXXX (Addr to Store Digit Input Group)	DI or PI Group to Core Storage	5A XX	-DI Addr 40 thru 7F or PI Addr 02 thru 19
Sense Device	0000	DSW, DI, or PISW A-register	5F 00 01 XX	-DSW -DSW, Reset Indicators -DI Addr 40 thru 7F or PISW Addr 02 thru 19
Control	0000	Generate Reset to DI Controls	5C20	
Data Channel Control Initialize Read	XXXX (Addr of Data Table)	Set up DC Controls for Transfer of Data	5E X0 8 9 10 11: 0 00 = Read Random 01 = Read Sequential 10 = Read Single 1 = Ex. Sync.	
Analog Input				
Direct Program Control Write	XXXX (Mpx Addr Location)	AI- AIE-	51 81 Analog Input to ADC XX 8 9 10 11 12 13 14 15: 00 000 00=11-bit res. 01 = 14-bit res. 10 = 8-bit res. 1 = Ex. Sync.	
Read	XXXX (Addr to Store ADC Reading)	AI- AIE-	52 82 ADC to Core 00 80	-Sequential Programmed Operation
Control	0000	AI- AIE-	5400 8400	Reset Controls and Registers
Sense Device	0000	AI- AIE-	57 87 0 8 1	-AI -Comparator -Reset Indicators

Device/Function	IOCC: Address Word (Hex.)	IOCC: Area, Function, and Modifier Word		
Analog Input Continued				
Data Channel Control Initialize Write	XXXX (First Mpx Addr Table Location)	AI- AIE-	5500 8500	(Set up DC for Transfer of Mpx Addr and Limit Words)
Initialize Read	XXXX (First Data Table Addr)	AI- AIE-	56 86 XX 8 9 10 11 12 13 14 15: 0 000 00 = 11-bit res. 01 = 14-bit res. 10 = 8-bit res. 0 = 1 DC Operation 1 = 2 DC Operation 1 = Ex. Sync.	
Digital and Analog Output				
Direct Program Control Write	XXXX (Addr of Output Data)	Core Storage to DAO Device	61 XX	-DAO Register Addr 00 thru 7F
Control	0000		64 20 40 80	-Reset DAO Controls -Initiate Simultaneous Transfer from Registers -Start Pulse Output Timer
Sense Device	0000	DSW to A A-register	6700 01	-Reset Indicators
Data Channel Control Initialize Write	XXXX (Addr of Data Table)	Set up DC Controls to Transfer Data	65 X0 8 9 10 11: 0 0 0 = Random 1 = Single 1 = Ex. Sync.	

IOCC Format



Interrupts

Interrupt	Priority Level	Core Storage Location Decimal	Core Storage Location Hex.	ILSW	
Internal	1	8	8	Yes	
Trace	26	9	9	No	
** CE	27	10	A	No	
*External 0	2	11	B	Yes	
1	3	12	C	Yes	
2	4	13	D	Yes	
3	5	14	E	Yes	
4	6	15	F	Yes	Basic
5	7	16	10	Yes	
6	8	17	11	Yes	
7	9	18	12	Yes	
8	10	19	13	Yes	
9	11	20	14	Yes	
10	12	21	15	Yes	
11	13	22	16	Yes	
12	14	23	17	Yes	
13	15	24	18	Yes	
14	16	25	19	Yes	Special
15	17	26	1A	Yes	Feature
16	18	27	1B	Yes	Group 1
17	19	28	1C	Yes	
18	20	29	1D	Yes	
19	21	30	1E	Yes	Special
20	22	31	1F	Yes	Feature
21	23	32	20	Yes	Group 2
22	24	33	21	Yes	
23	25	34	22	Yes	

* External Interrupt cannot occur at the end of an XIO or BSI instruction.

** A CE Interrupt Stores the return link in core location 10 (decimal) and starts execution at core location 0001. Interrupts are prevented in the same manner as for the standard forced BSI.

Instruction Set

Hexadecimal	Branch Instructions
BE00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR2) and EA+1
BF00XXXX	Compare A and Q with contents of CSL at EA (Addr+XR3) and EA+1
BC80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at Addr) and EA+1
BD80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr +XR1") and EA+1
BE80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr +XR2") and EA+1
BF80XXXX	Compare A and Q with contents of CSL at EA (V in CSL at "Addr +XR3") and EA+1
	I/O Instructions
	Execute I/O (XIO)
08XX	Execute IOCC in CSL at EA (I+DISP) and EA+1
09XX	Execute IOCC in CSL at EA (XR1+DISP) and EA+1
0AXX	Execute IOCC in CSL at EA (XR2+DISP) and EA+1
0BXX	Execute IOCC in CSL at EA (XR3+DISP) and EA+1
0C00XXXX	Execute IOCC in CSL at EA (Addr) and EA+1
0D00XXXX	Execute IOCC in CSL at EA (Addr+XR1) and EA+1
0E00XXXX	Execute IOCC in CSL at EA (Addr+XR2) and EA+1
0F00XXXX	Execute IOCC in CSL at EA (Addr+XR3) and EA+1
0C80XXXX	Execute IOCC in CSL at EA (V in CSL at Addr) and EA+1
0D80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR1") and EA+1
0E80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR2") and EA+1
0F80XXXX	Execute IOCC in CSL at EA (V in CSL at "Addr+XR3") and EA+1

Symbol	Meaning
A	Accumulator
Q	Accumulator Extension
Addr	Contents of the address portion of a two-word instruction
CSL	Core storage location
DISP	Contents of the displacement portion of a one-word instruction
EA	Effective address (See Figure 1-)
EA + 1	Next higher address from the effective address
I	Contents of the Instruction Register
V	Value
XR1	Contents of Index Register 1
XR2	Contents of Index Register 2
XR3	Contents of Index Register 3
X	Hexadecimal value can be 0-F
*	Used for hexadecimal values that have limits

Effective Address Computation

Tag Bits	F = 0 (Direct Addressing)	F = 1, IA = 0 (Direct Addressing)	F = 1, IA = 1 (Indirect Addressing)
T = 00	EA = I + Disp	EA = Address	EA = C (Address)
T = 01	EA = XR1 + Disp	EA = Address + XR1	EA = C (Address + XR1)
T = 10	EA = XR2 + Disp	EA = Address + XR2	EA = C (Address + XR2)
T = 11	EA = XR3 + Disp	EA = Address + XR3	EA = C (Address + XR3)

Disp = Contents of Displacement field of instruction
C = Contents of location specified by Address or Address + XR1, 2 or 3

Device Status Words

Internal Interrupt ILSW

0	1	2	3	
Invalid Op Code	Parity Error	Storage Protect Violation	CAR Check Error	(No others used.)

AREA	FEATURE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Console Interrupt	* Interrupt Request															
	Interval Timers	* Timer A	* Timer B	* Timer C													
	Data Entry Switches	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	Sense Switches	← Sense →				← Program →				← CE Sense →							
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1- 15-	1816 Printer-Keyboard 1053 Printer -In First Group -In Second Group	* Printer Service Response	* Keyboard Service Response (1816)	* Keyboard Request (1816)		Printer Busy	Printer Not Ready	Keyboard Not Ready	Storage Protect Violation (1816)	Keyboard Parity Error (1816)	Printer Parity Error			†CE Busy	†CE Not Ready		
2- 17-	1442 Card Read Punch -First -Second			Error	Last Card	* Operation Complete	Parity Error	Storage Protect Violation	Feed Check Read Station					†CE Busy	†CE Not Ready	Busy	Not Ready
3	1054/1055 Paper Tape Reader/Punch	PT Reader Any Error	* PT Reader Service Request	PT Punch Parity Error	* PT Punch Service Request	PT Reader Busy	PT Reader Not Ready	PT Punch Busy	PT Punch Not Ready	PT Reader Parity Error	PT Reader Storage Protect	†CE PT Reader Busy	†CE PT Reader Not Rdy	†CE PT Punch Busy	†CE PT Punch Not Rdy		
4- 8- 9-	1810 Disk Storage "A" First Drive Second Drive Third Drive	Any Error	* Operation Complete	Disk Not Ready	Disk Busy (R/W or Ctrl)	Carriage Home	Parity Error	Storage Protect Error	Data Error	Write Select Error	Data Overrun		†CE Not Ready	†CE Busy		Sector Count High	Sector Count Low
4- 8- 9-	1810 Disk Storage "B" First Drive Second Drive Third Drive	Any Error	* Operation Complete	Disk Not Ready	Disk Busy (R/W or Ctrl)	Carriage Home	Parity Error	Storage Protect Error	Data Error	Write Select Error	Data Overrun	Seek Error	†CE Not Ready	†CE Busy	"C" Model Access	Sector Count High	Sector Count Low
5	1627 Plotter	* Service Response	Parity Error											†CE Busy	†CE Not Ready	Busy	Not Ready
6	1443 Printer	* Transfer Complete	Error	* Printer Complete	Channel 9	Channel 12	Channel 1	Parity				†CE Carriage Busy	†CE Printer Busy	†CE Printer Not Ready	Carriage Busy	Printer Busy	Printer Not Ready
10- 16-	Analog Input -Basic -Expander	* End of Table	* DPC SS Conv Complete	* DPC Rly Conv Complete	* Storage Protect Violation	* Parity Control Error	* Parity Data Error	* Overload	* Overlap Conflict	Cyc Steal SS, AMAR Busy	DPC Relay Busy						Any Error
10- 16-	Comparator -AI Basic -AI Expander	* High Out of Limit	* Low Out of Limit	* Overload	AMAR SS MPX			AMAR 512	AMAR 256	AMAR 128	AMAR 64	AMAR 32	AMAR 16	AMAR 8	AMAR 4	AMAR 2	AMAR 1
11	Digital Input	* Parity Error	* Storage Protect Violation	* DI Scan Complete	* Command Reject												DI Busy
	PISW	← Process Interrupt Points (Customer Assigned Groups) →															
12	Digital and Anolog Output	* Parity Error	Pulse Output Timer	* D & A Out Scan Complete	* Command Reject	Data Channel Active											D/AO Busy
13	S/360 Adapter	* Command Reject	1800 Command Stored	* 360 Command Stored	* Halt	* Data Check	* Storage Protect Violation	* Transfer End	* End of Table	← 360 Command Byte →							
	Adapter Word Counter			← Word Count (1's Complement) →													
14	Tape Control Unit		Tape Unit 1 Select	* Command Reject	* End of Table	Chain Stop	Storage Protect Violation Stop	Tape Data Error	Data Bus Out or P-C Parity Error	Data Overrun Error	* Operation Complete	CE Diagnostic Indicator	Wrong Length Record	At Load Point	Tape Indicator or Mark	Tape Busy or Rewind	Tape Busy or Not Ready
	TCU Word Counter	00 = True Count 11 = 1's Complement	← Word Count →														

* Interrupt Conditions
† Active Only in CE Mode

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